CLAIMS

1. A bias circuit for an amplifier, said bias circuit comprising:

a first bipolar transistor having a base connected to a first node, said first node connected to a reference voltage through a first resistor;

a second bipolar transistor having a base connected to said first node;

a third bipolar transistor having a collector connected to said first node and a base connected to an emitter of said first bipolar transistor at a second node, an emitter of said second bipolar transistor being connected to a base of a fourth bipolar transmitter associated with said amplifier, said second bipolar transistor not having a resistor connected to said emitter of said second bipolar transistor.

2. The bias circuit of claim 1, wherein an emitter size ratio of said first bipolar transistor to said second bipolar transistor is independent of an emitter size ratio of said third bipolar transistor to said fourth bipolar transistor.

3. The bias circuit of claim 1, further comprising a control circuit connected to said second node, said control circuit drawing an increased current during a high mode operation and drawing a reduced current during a low mode operation.

4. The bias circuit of claim 3, wherein said control circuit has a reduced resistance during said high mode operation and an increased resistance during said low mode

operation.

5. The bias circuit of claim 3, wherein said control circuit comprises a fifth bipolar transistor having a collector connected to said second node through a second resistor and to ground through a third resistor, an emitter of said fifth bipolar transistor being coupled to ground, and a base of said fifth bipolar transistor connected to a control voltage through a fourth resistor.

6. The bias circuit of claim 1, further comprising a high-temperature gain compensation circuit connected in parallel with said first resistor, said high-temperature gain compensation circuit configured to draw current at high temperatures.

7. The bias circuit of claim 6, wherein said high-temperature gain compensation circuit comprises a second resistor and a Schottky diode, wherein a first end of said second resistor is connected to said reference voltage, a second end of said second resistor being connected to an anode of said Schottky diode, and a cathode of said Schottky diode being connected to said first node.

8. A control circuit for the operation of a bias circuit, said bias circuit including a first bipolar transistor, a second bipolar transistor, and a third bipolar transistor, said first bipolar transistor having a base connected to a base of said second bipolar transistor at a

first node, said first node connected to a reference voltage through a first resistor, said third bipolar transistor having a collector connected to said first node and a base connected to an emitter of said first bipolar transistor at a second node, an emitter of said second bipolar transistor being connected to a base of a fourth bipolar transmitter associated with said amplifier, said control circuit comprising:

a fifth bipolar transistor having a collector connected to said second node through a second resistor and to ground through a third resistor, an emitter of said fifth bipolar transistor being coupled to ground, and a base of said fifth bipolar transistor connected to a control voltage through a fourth resistor.

9. The control circuit of claim 8, wherein said control circuit draws an increased current during a high mode operation and draws a reduced current during a low mode operation

10. The control circuit of claim 9, wherein during said high mode operation, said control circuit has said total resistance equivalent to said second resistor.

11. The control circuit of claim 9, wherein during said low mode operation, said control circuit has a total resistance equivalent to the sum of said second resistor and said third resistor.

12. The control circuit of claim 9, wherein said fifth bipolar transistor is deactivated during said low mode operation, and said fifth bipolar transistor is activated during said high mode operation.

13. The control circuit of claim 8, wherein said second bipolar transistor does not have a resistor connected to said emitter of said second bipolar transistor.

14. An amplifier circuit comprising:

a bias circuit including a first bipolar transistor, a second bipolar transistor, and a third bipolar transistor, said first bipolar transistor having a base connected to a base of said second bipolar transistor at a first node, said first node connected to a reference voltage through a first resistor, said third bipolar transistor having a collector connected to said first node and a base connected to an emitter of said first bipolar transistor at a second node, said second bipolar transistor not having a resistor connected to said emitter of said second bipolar transistor;

an amplifier including a fourth bipolar transmitter having a base connected to an emitter of said second bipolar transistor, and an emitter coupled to ground.

15. The amplifier circuit of claim 14, wherein an emitter size ratio of said first bipolar transistor to said second bipolar transistor is independent of an emitter size ratio of said third bipolar transistor to said fourth bipolar transistor.

16. The amplifier circuit of claim 14, further comprising a control circuit connected to said second node, said control circuit drawing an increased current during a high mode operation and drawing a reduced current during a low mode operation.

17. The amplifier circuit of claim 16, wherein said control circuit has a reduced resistance during said high mode operation and an increased resistance during said low mode operation.

18. The amplifier circuit of claim 16, wherein said control circuit comprises a fifth bipolar transistor having a collector connected to said second node through a second resistor and to ground through a third resistor, an emitter of said fifth bipolar transistor being coupled to ground, and a base of said fifth bipolar transistor connected to a control voltage through a fourth resistor.

19. The amplifier circuit of claim 14, further comprising a high-temperature gain compensation circuit connected in parallel with said first resistor, said high-temperature gain compensation circuit configured to draw current at high temperatures.

20. The amplifier circuit of claim 19, wherein said high-temperature gain compensation circuit comprises a second resistor and a Schottky diode, wherein a first

end of said second resistor is connected to said reference voltage, a second end of said second resistor being connected to an anode of said Schottky diode, and a cathode of said Schottky diode being connected to said first node.